

DAOS 2.4 and Beyond

Johann Lombardi, Senior Principal Engineer, AXG, Intel
6th DAOS User Group, Dallas, Nov 22, 2022



intel[®]

Notices and Disclaimers

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration.

No product or component can be absolutely secure.

Tests document performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. For more complete information about performance and benchmark results, visit <http://www.intel.com/benchmarks>.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit <http://www.intel.com/benchmarks>.

Intel Advanced Vector Extensions (Intel AVX) provides higher throughput to certain processor operations. Due to varying processor power characteristics, utilizing AVX instructions may cause a) some parts to operate at less than the rated frequency and b) some parts with Intel® Turbo Boost Technology 2.0 to not achieve any or maximum turbo frequencies. Performance varies depending on hardware, software, and system configuration and you can learn more at <http://www.intel.com/go/turbo>.

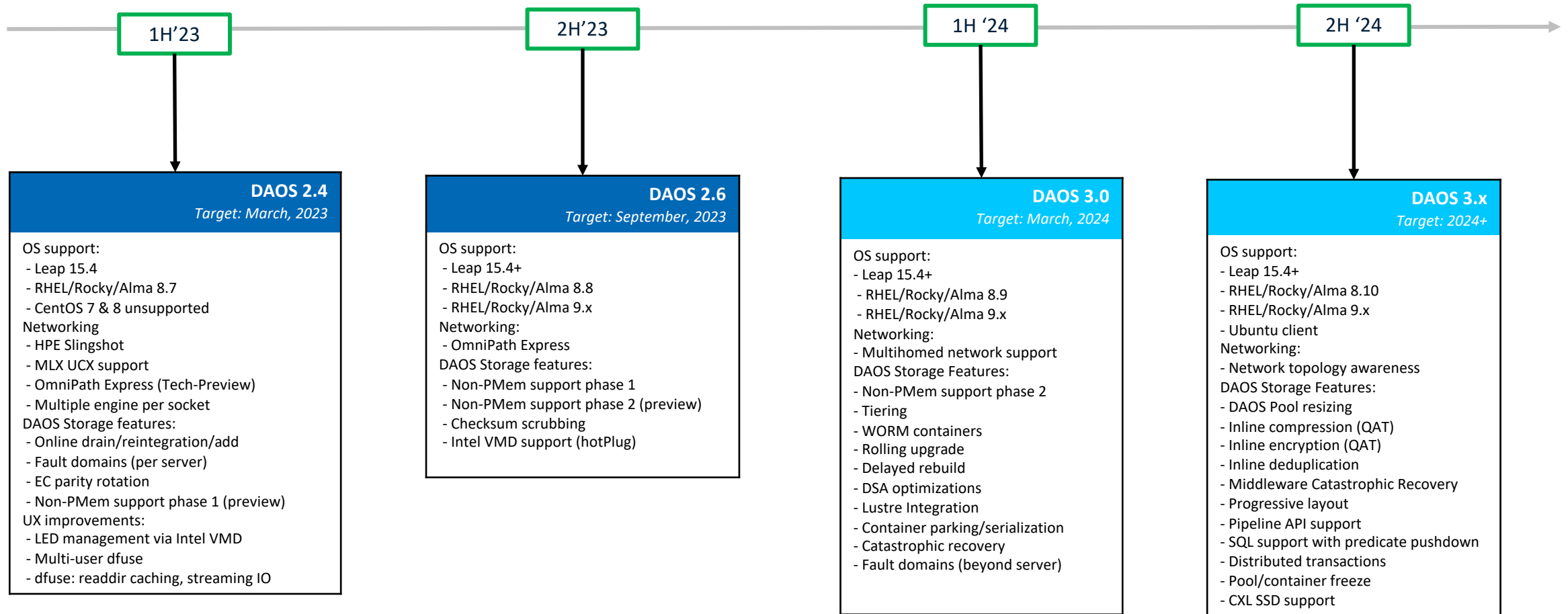
Intel's compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice.

Cost reduction scenarios described are intended as examples of how a given Intel-based product, in the specified circumstances and configurations, may affect future costs and provide cost savings. Circumstances will vary. Intel does not guarantee any costs or cost reduction.

Intel does not control or audit third-party benchmark data or the web sites referenced in this document. You should visit the referenced web site and confirm whether referenced data are accurate.

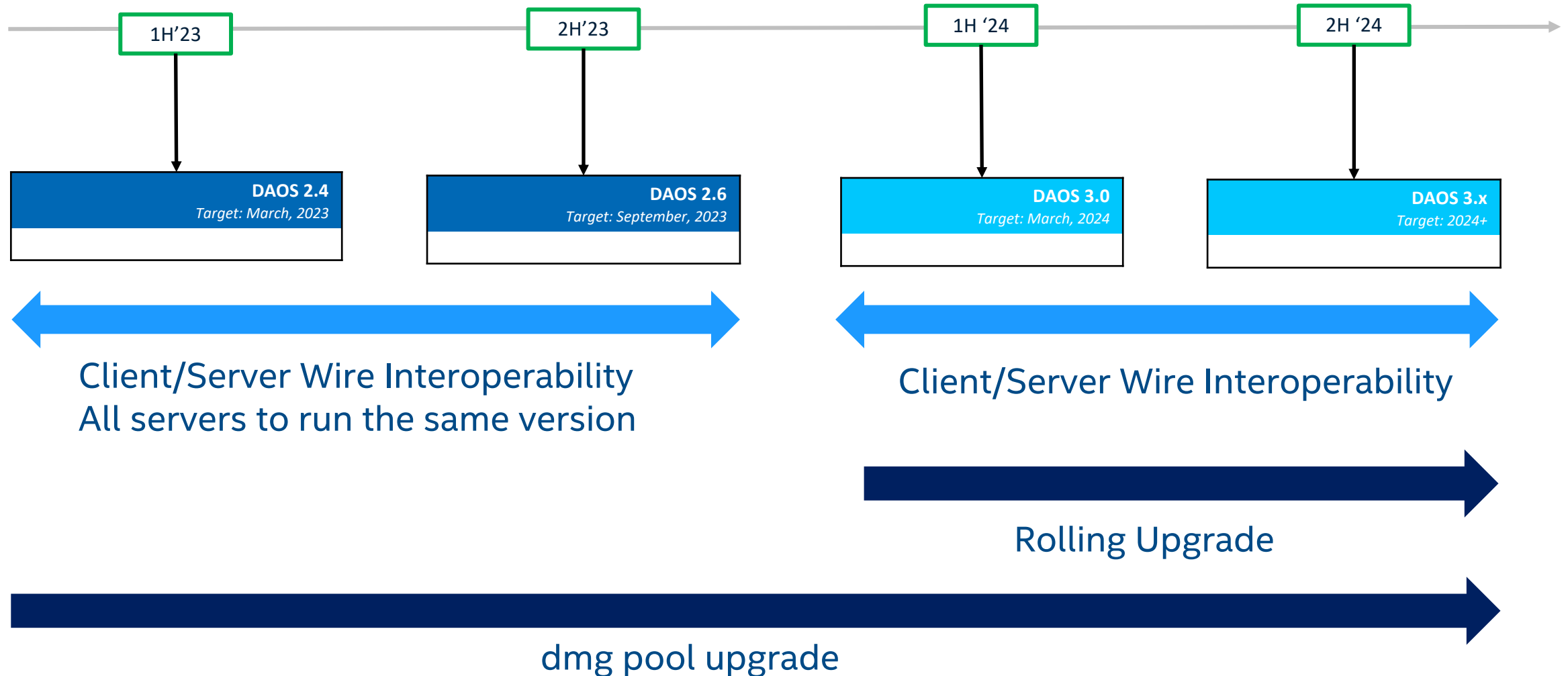
© Intel Corporation. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Other names and brands may be claimed as the property of others.

DAOS Upcoming **Community** Releases



NOTE: All information provided in this roadmap is subject to change without notice.

Interoperability / Upgradability



Network: Buffer Mgmt Improvements (2.4)

- Enable MR (memory registration) cache
 - Required for CXI support
 - Dfuse changes to be MR cache-friendly in progress
- OFI MULTI_RECV support
 - Faced issue with buffer exhaustion at larger scale
 - Change Mercury to support OFI multi-recv API
 - Post large buffers where incoming messages are appended
 - Protocol changes since no tag support
 - Supported by most providers

Network: UCX Support (2.4)

- Mellanox UCX library
- Future path for MLX HW support:
 - Shipped as part of MOFED packages
 - Better scalability on MLX fabric via DC & UD support
 - Native multi-rail support
 - GDS support on MLX/NVIDIA HW
- Should eventually replace OFI verbs provider
- Feature preview in 2.2 and official support in 2.4
- More work to be done to demonstrate scalability

DAOS

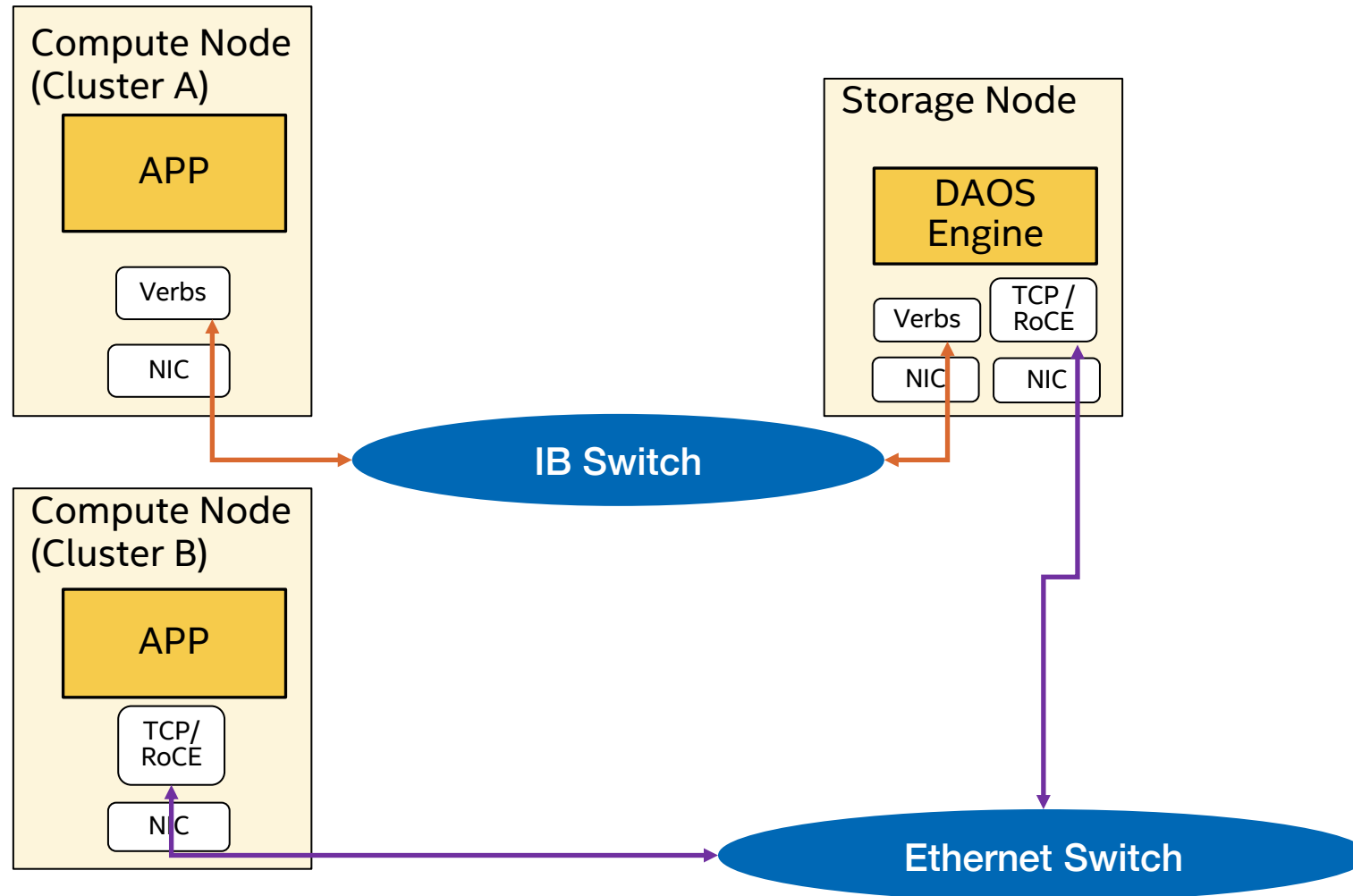
CART

Mercury

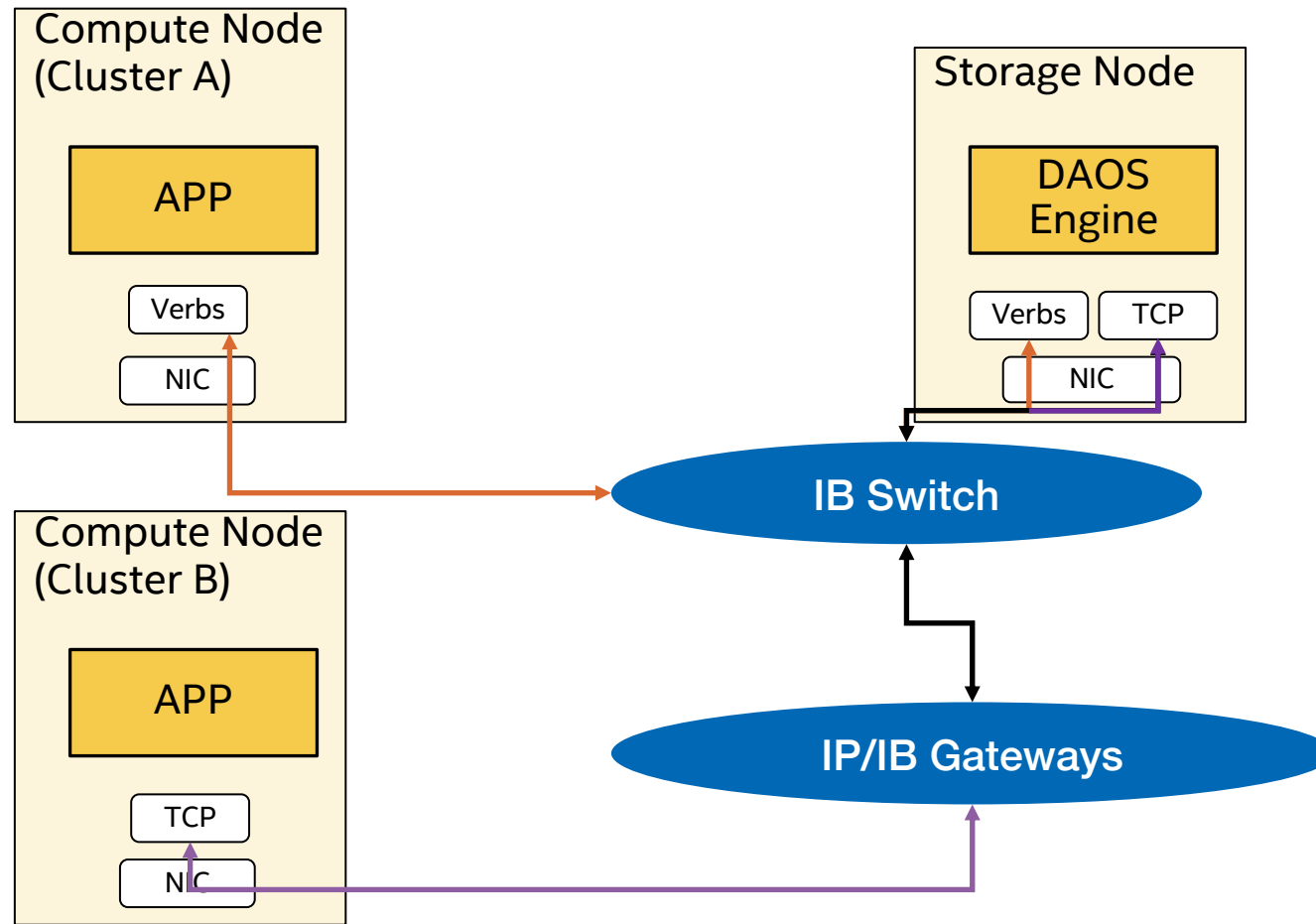
OFI

UCX

Network: Multi-Homed Network (3.0)



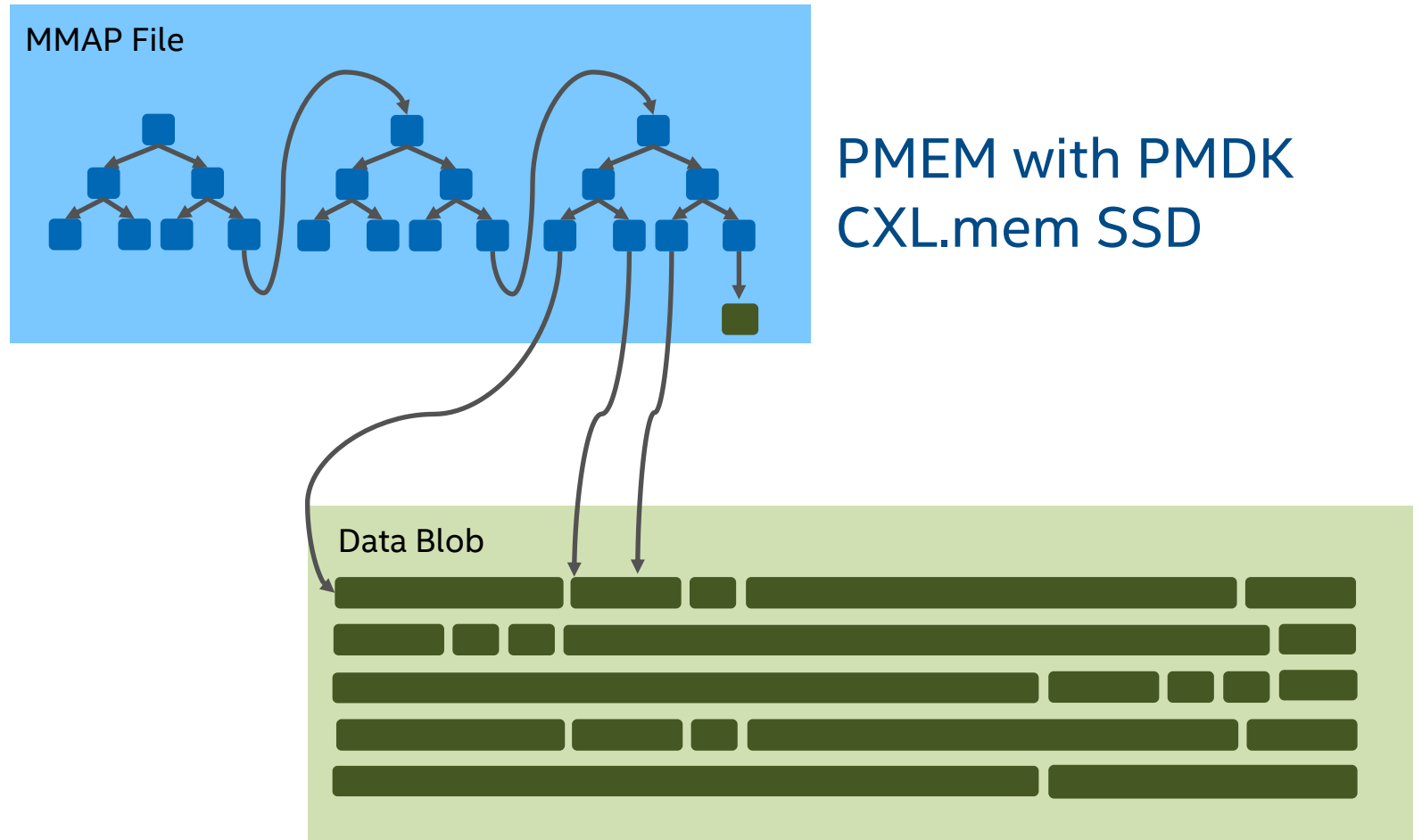
Network: Multi-Homed Network (3.0)



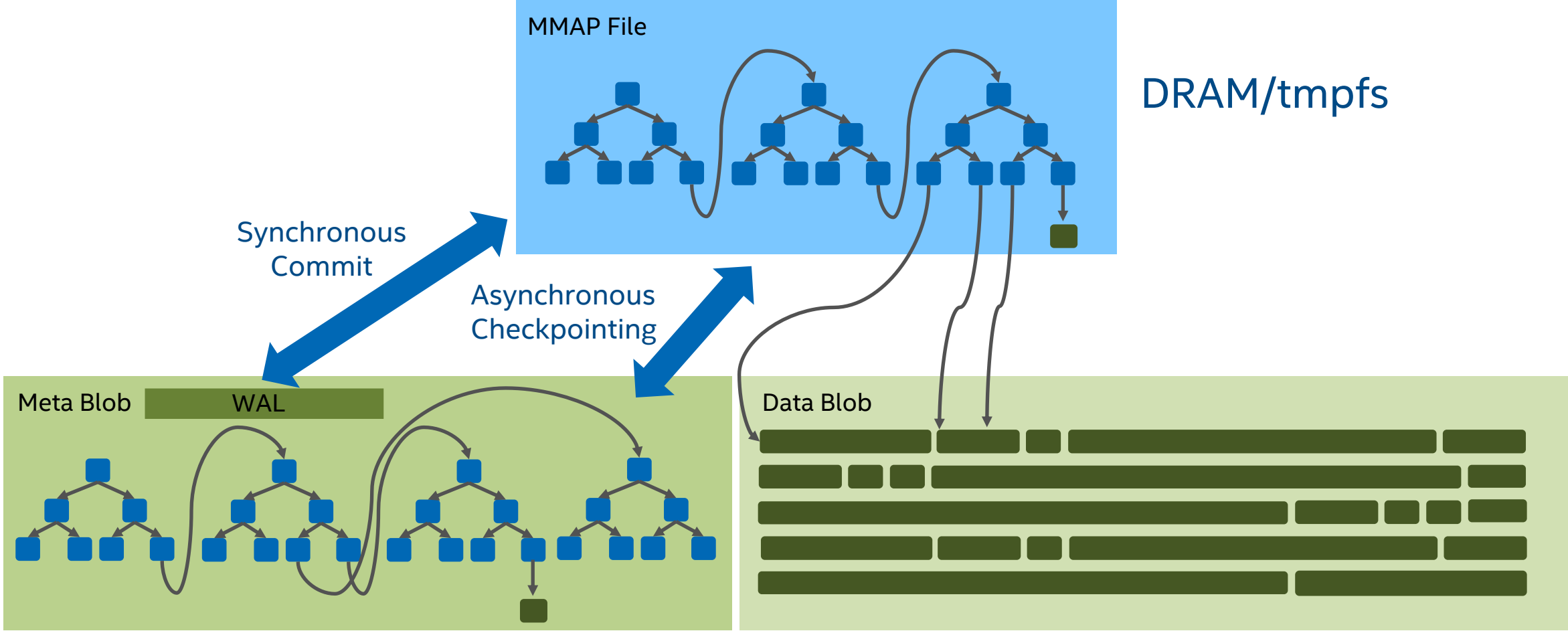
Backend: Metadata on SSD Requirements (2.4+)

- Incremental changes
 - Deliver incremental functionality w/o waiting for another 4y
- Offer continuity to our current and future customers
- Maintain performance leadership
- Turn this into an opportunity to:
 - Strengthen the DAOS open-source community
 - Run DAOS on a wider range of hardware
 - Broaden the DAOS market
- <https://daosio.atlassian.net/wiki/spaces/DC/pages/11196923911/Metadata+on+SSDs>

Backend: Persistent Memory

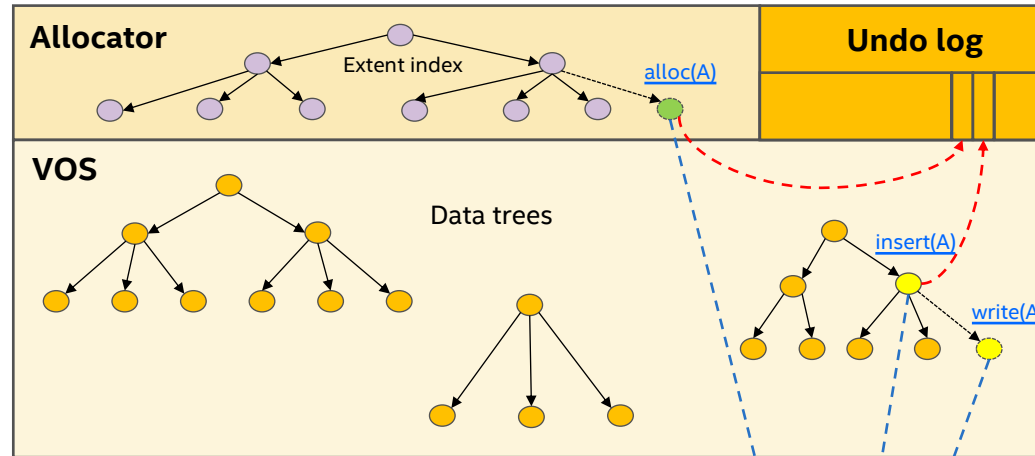


Backend: Volatile Memory



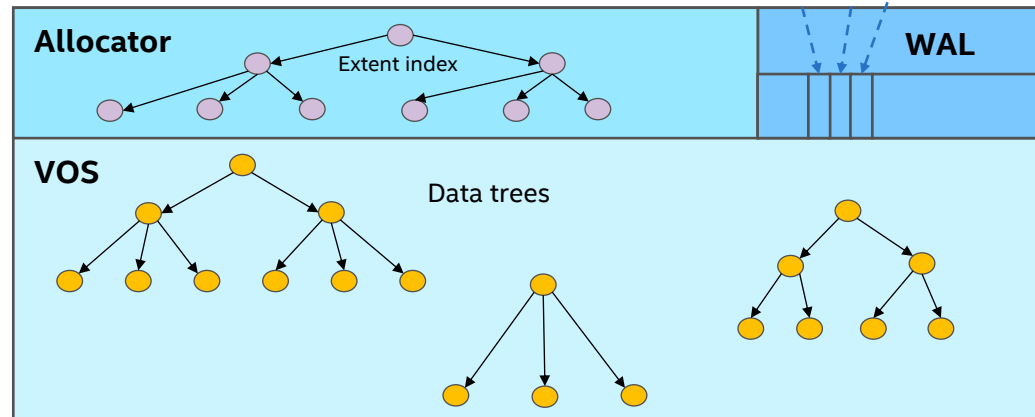
Backend: New (Meta)Data Structures

md.mem



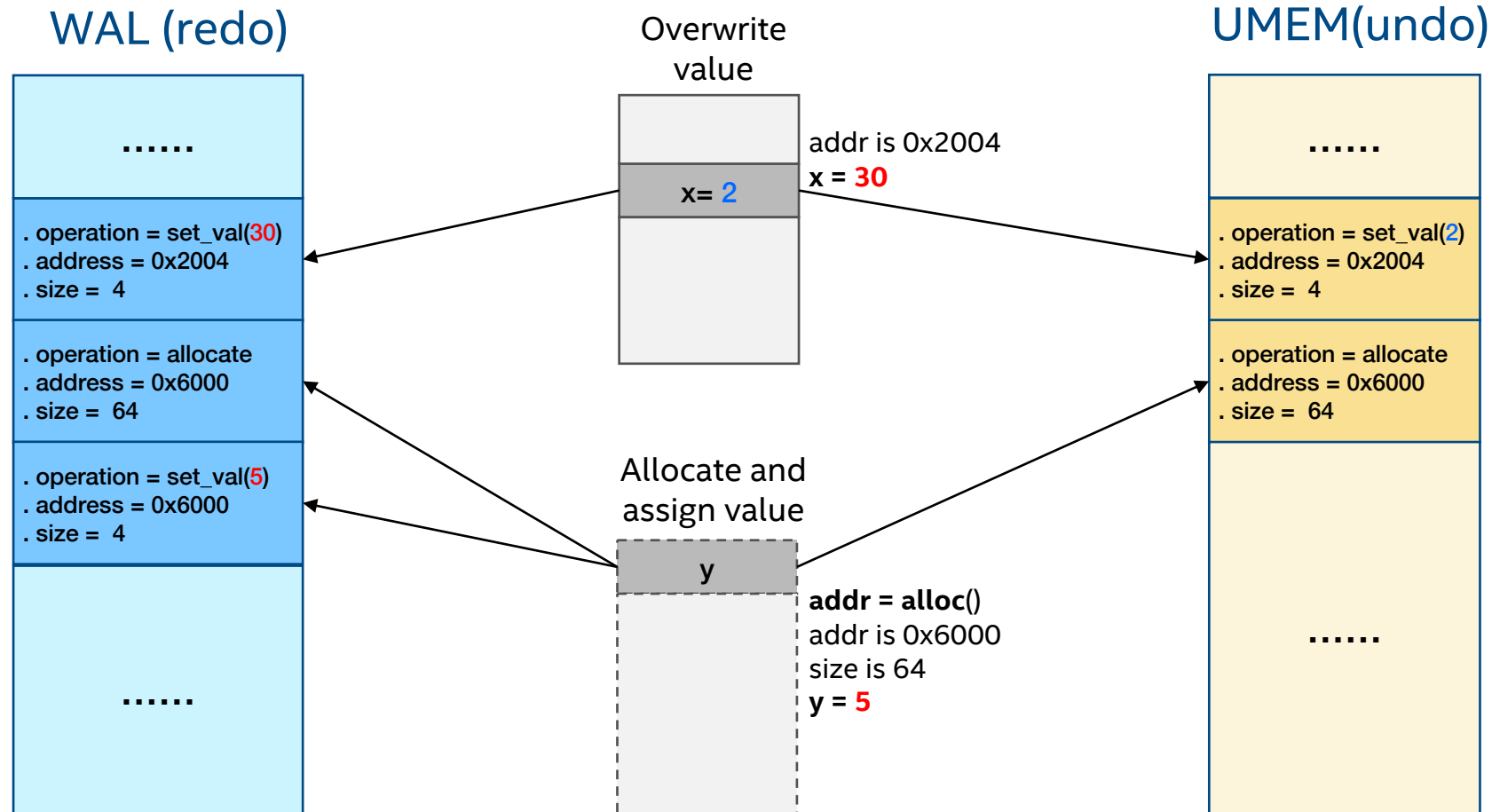
Undo log is **off-heap**, it has no persistent mirror

md.blob

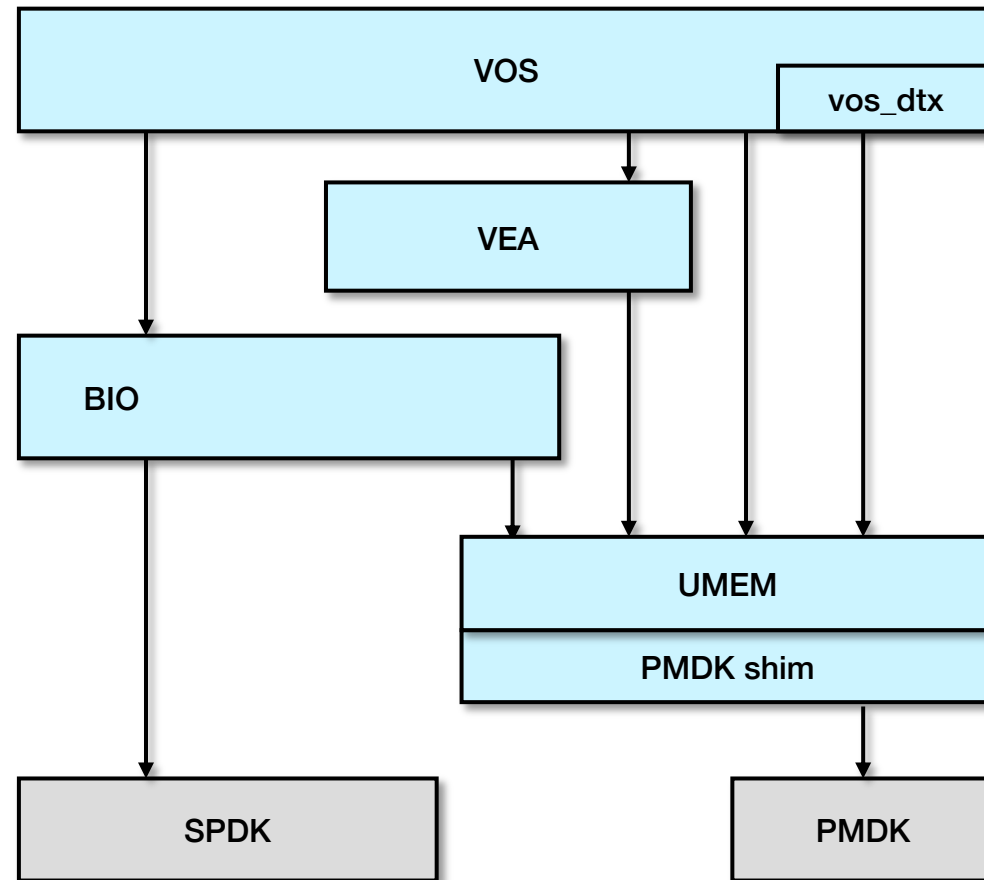


WAL is on-heap (**or in a separate blob**), it has no ephemeral mirror.

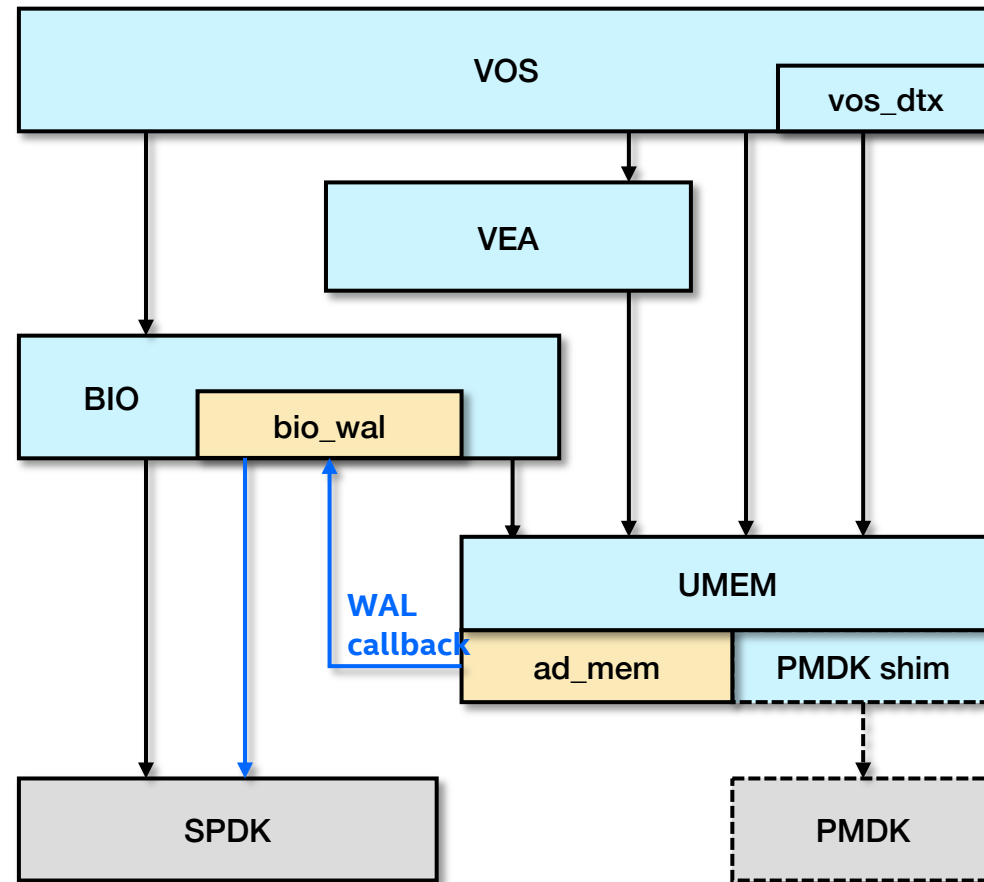
Backend: Undo vs Redo



Backend: Stack Layering (2.2)

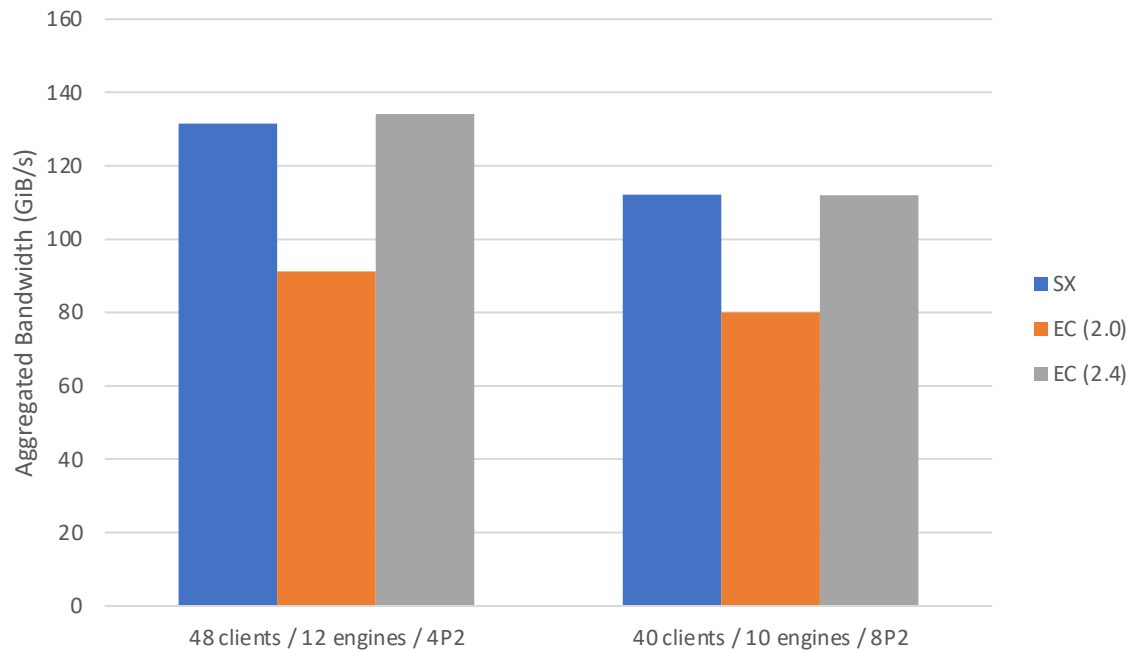


Backend: Stack Layering (2.4+)

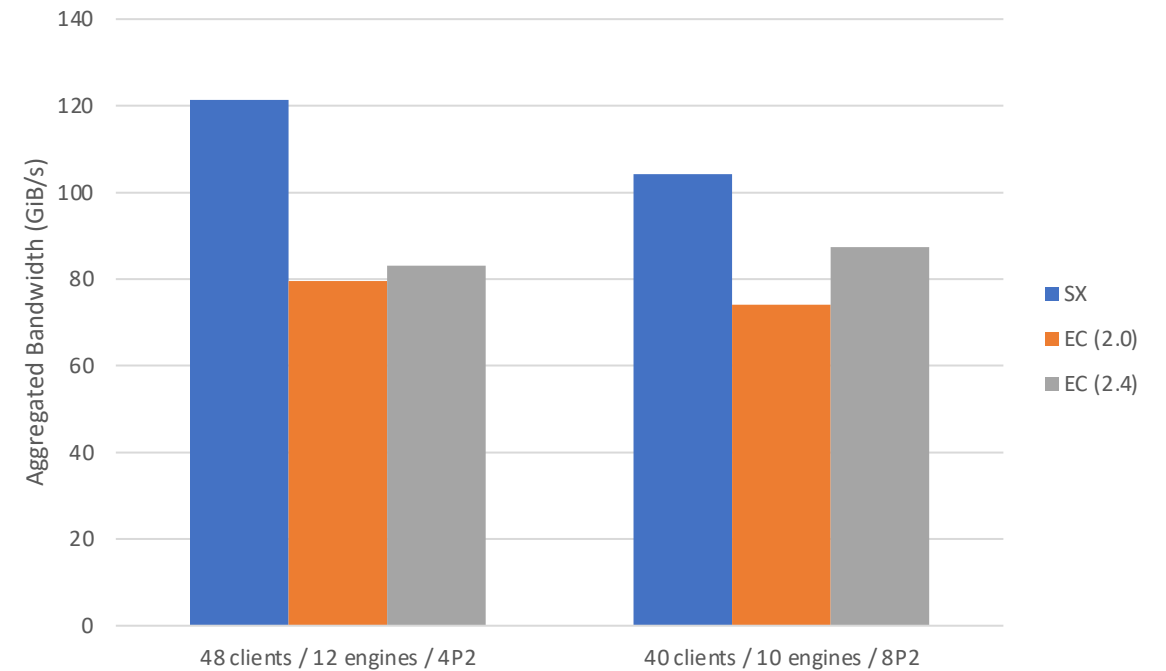


Erasure Code: Parity Rotation (2.4)

IOR Easy Read



IOR Easy Write



Middleware: State of Affairs



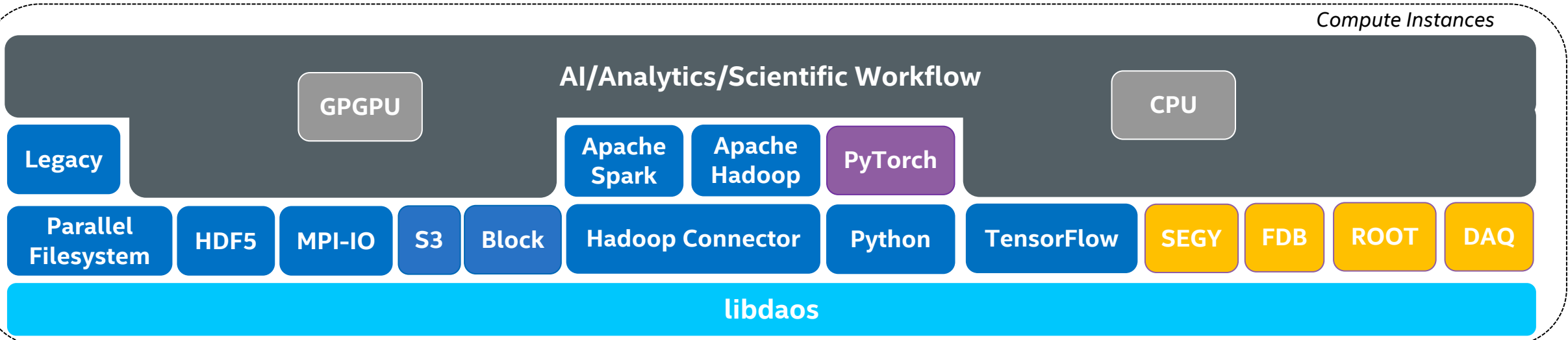
python



PyTorch



TensorFlow



Native array



Native key-value



RDMA



Generic I/O middleware supported today



Domain-specific data models under development in co-design with partners



Enablement in progress

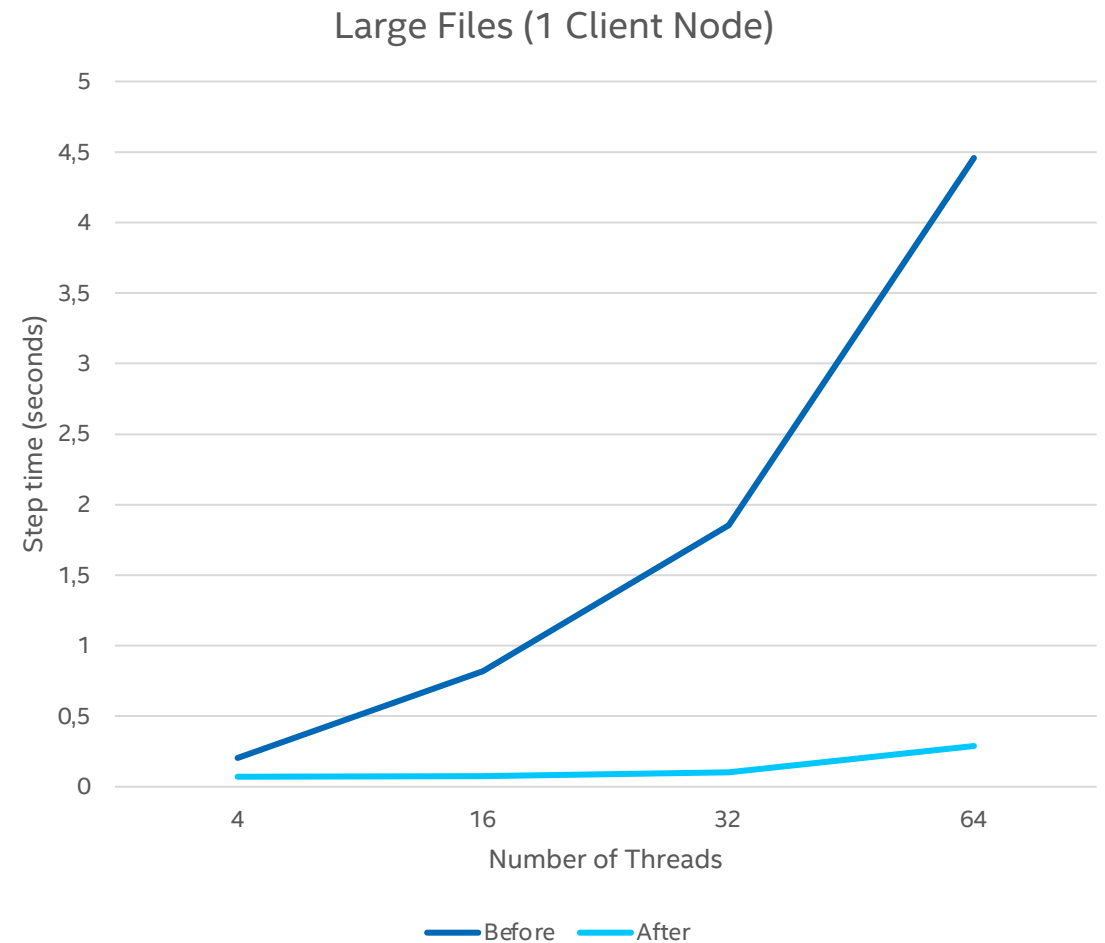
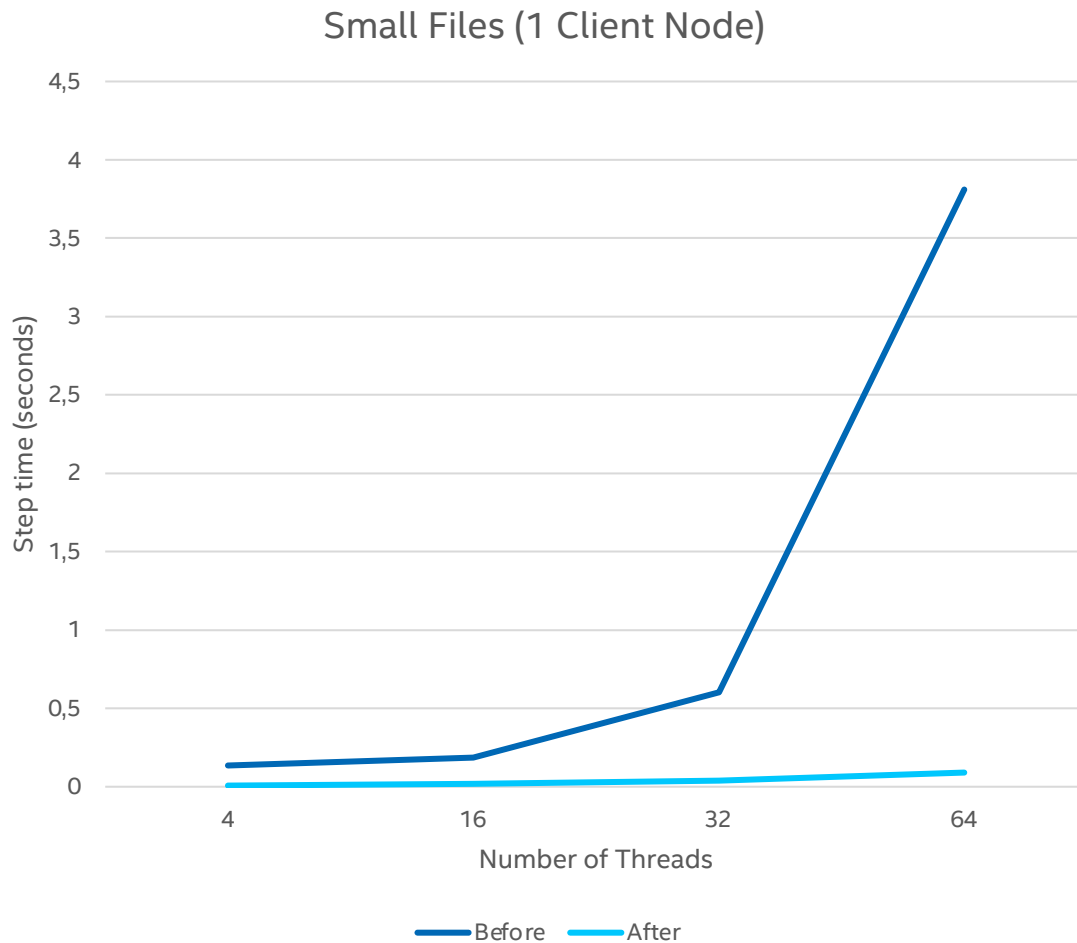
Middleware: dfuse & IL Improvements (2.4)

- Multi-user dfuse
 - Mountpoint owned by root and accessible by all users
 - Unix permissions apply
 - Can be used with IL, but no global handle
- Interception of streaming functions
 - `f{open,read,write,close,...}`
 - No caching
- Aggressive dfuse caching
 - Readdir and other operations

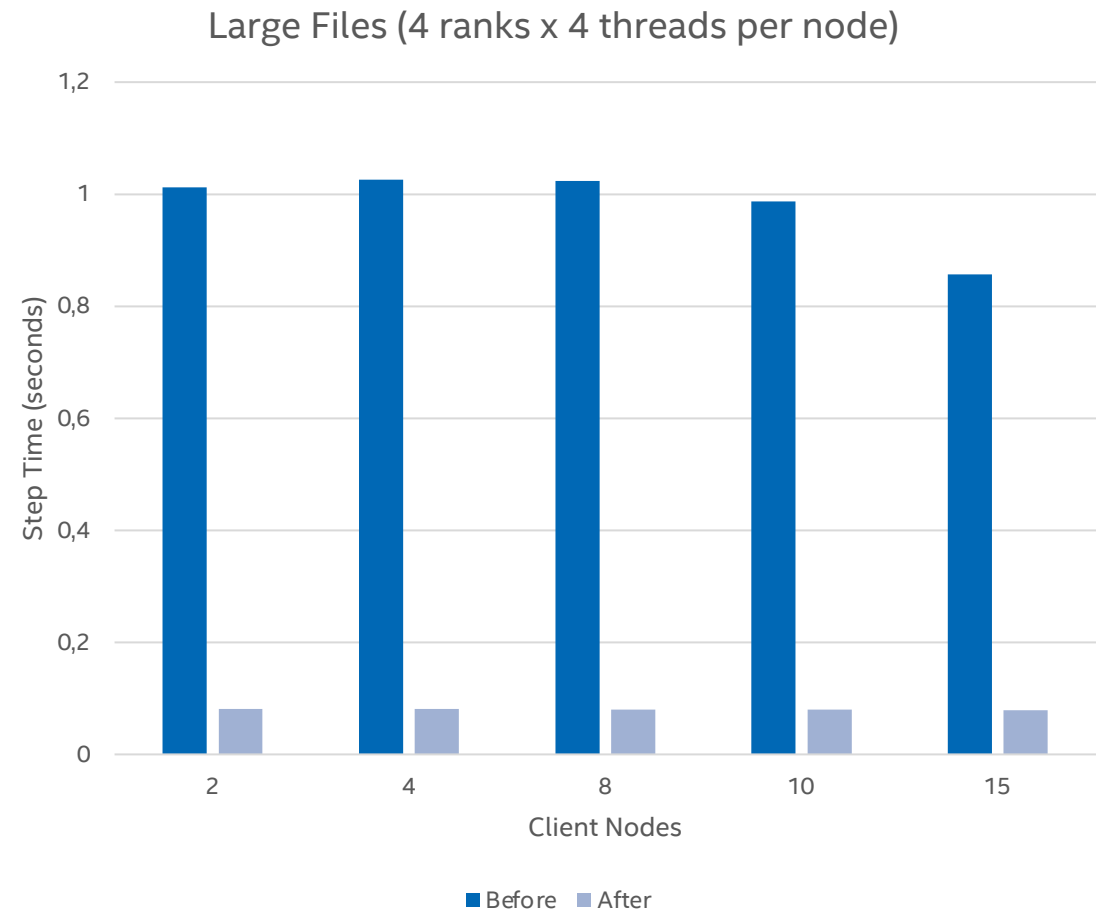
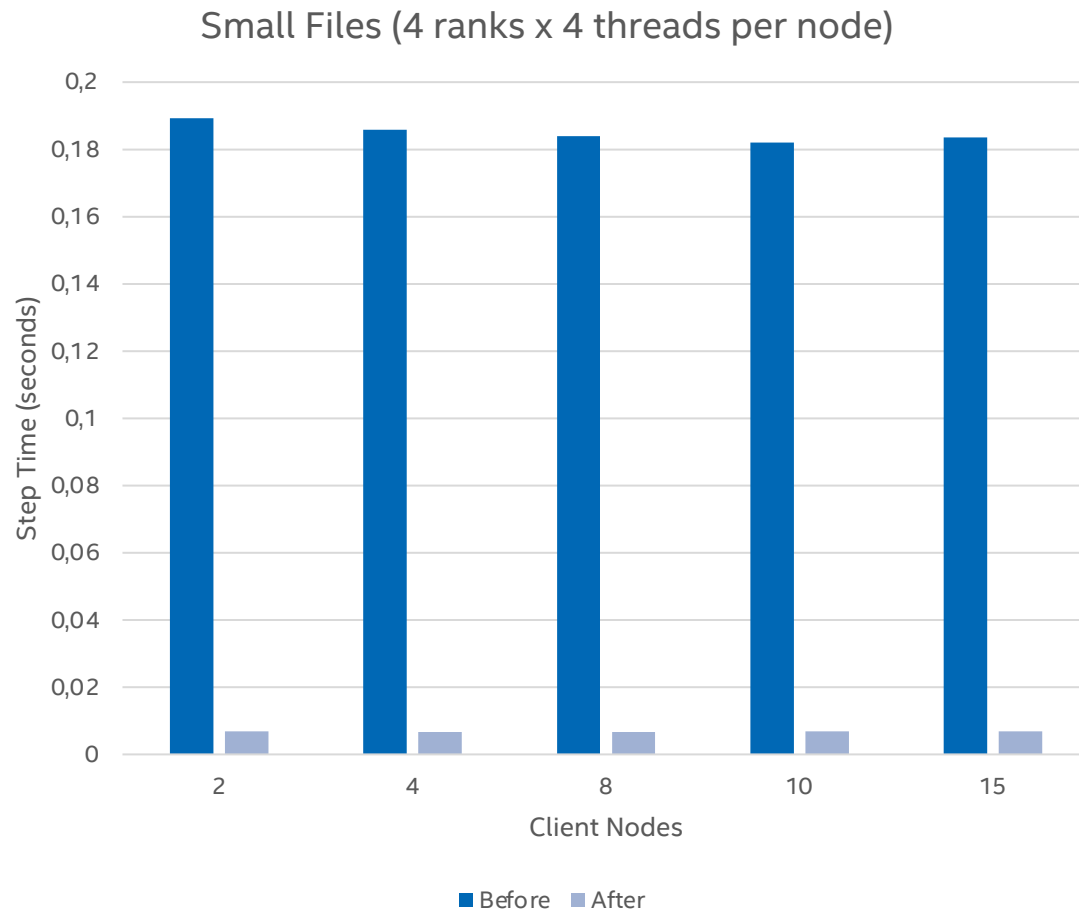
Middleware: dfuse Caching AI Benchmark

- Benchmark to simulate some AI / ML workloads
 - 2 Datasets: large number of 4k files, small number of 4m files
 - x MPI ranks, each having y threads, all reading the dataset at the same time
 - Stat, open, read, close
- Measure on wolf using dfuse:
 - Before results: all default options
 - After results: do all the optimizations for aggressive caching
- Benchmark from LRZ: Durillo Barrionuevo, Juan; Hammer, Nicolay

Middleware: dfuse Caching 1 Client



Middleware: dfuse Caching Many Clients



Middleware: WORM Containers (3.0)

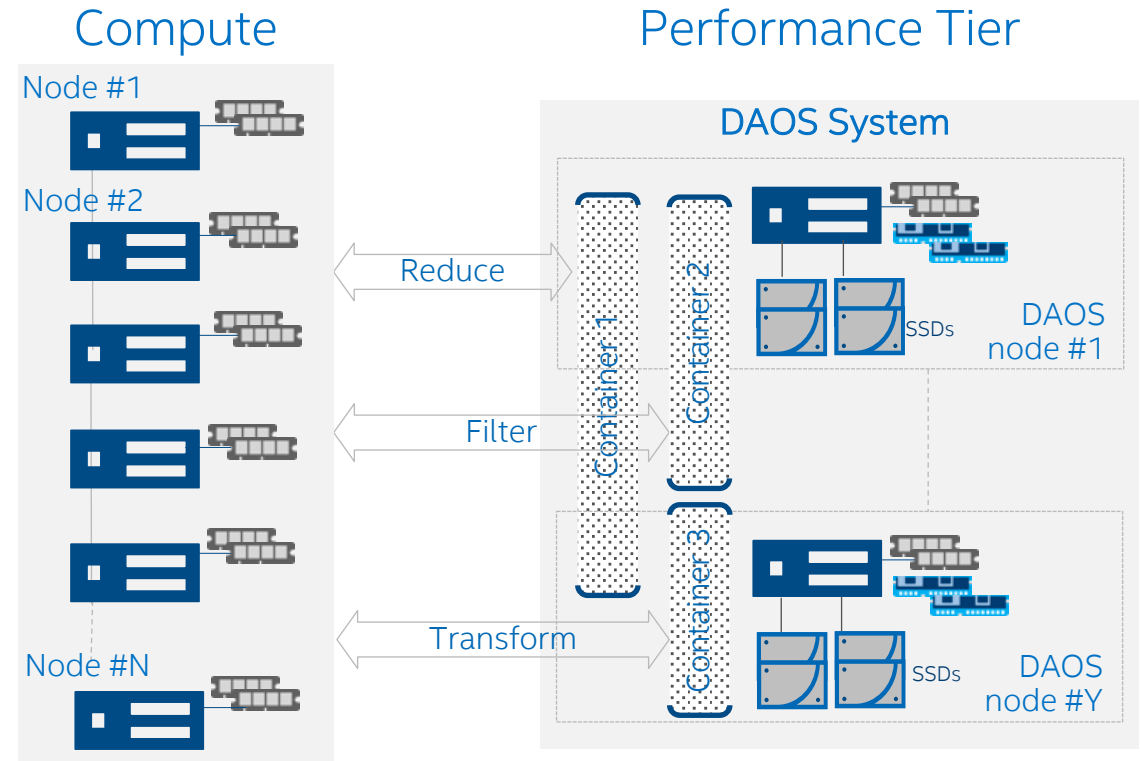
- Write Once Read Many Containers
- Optimizations for read-only datasets
 - Aggressive caching
 - Read-optimized layout
 - Size optimizations for immutable files
 - Indexing
- Use cases
 - Training/verification datasets

Direction: Full Userspace POSIX Support

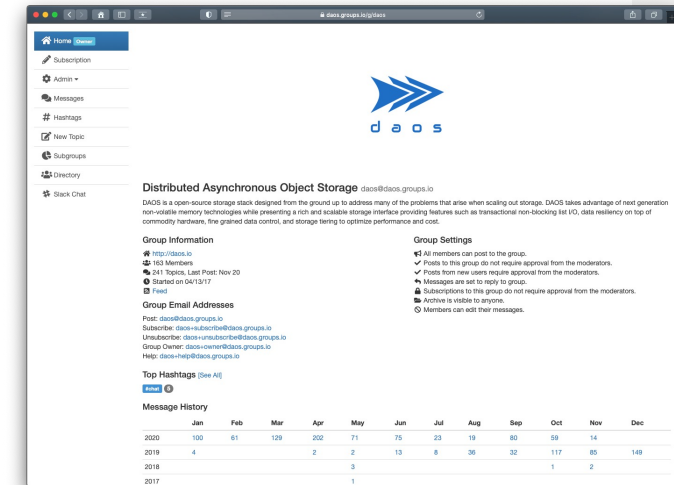
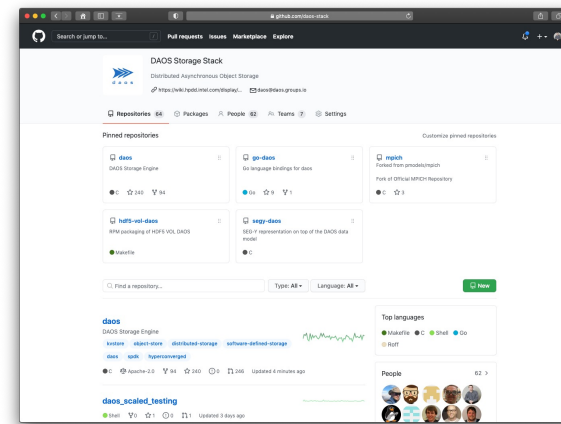
- Intercept **all** POSIX calls, including metadata operations
 - File open/create/stat/close and derivative
 - mmap via userfaultfd
- **Collaborative** caching
 - Use shared memory for data & metadata caching
 - Accessible by all ranks running on the same node
 - Size of cache configurable

Direction: Scale-out Active Storage

- DAOS pipeline API
 - Offload data-intensive processing to storage
 - Pre-defined or user-defined (ubpf)
- Leverage HW acceleration
 - computational storage devices
 - accelerators/smartNICs
- Many use cases
 - POSIX find(1)
 - SQL query / MariaDB prototype using predicate push-down
 - In-place data filtering/pre-processing/transformation for AI frameworks
 - Calculate max/min/sum/avg ... or searching for specific pattern/value on metadata/data



Resources



■ Open-source Community

- Github: <https://github.com/daos-stack/daos>
- Online doc: <http://daos.io>
- Mailing list & slack: <https://daos.groups.io>
- YouTube channel: <http://video.daos.io>

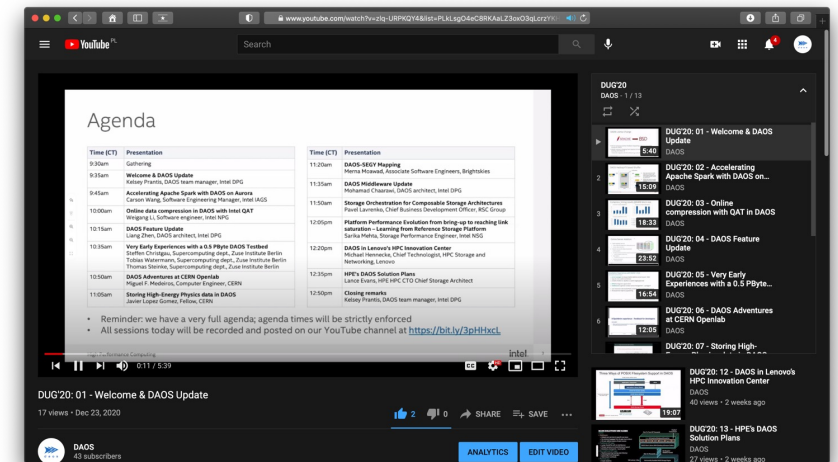
■ 6th DAOS User Group (DUG'22)

- Recordings will be available at <http://dug.daos.io>

■ DAOS BoF Community at SC'22

■ Intel landing page

- <https://www.intel.com/content/www/us/en/high-performance-computing/daos.html>



The Intel logo is centered on a solid blue background. It consists of the word "intel" in a white, lowercase, sans-serif font. A small blue square is positioned above the letter "i". To the right of the word "intel" is a registered trademark symbol (®) enclosed in a white circle.

intel®